

**TITLE : IMPEDANCE MODULATION SIGNALLING**

This application is a continuation of International application  
5 No. PCT/GB99/00008, filed January 11, 1999.

**DESCRIPTION**

**FIELD OF THE INVENTION**

This invention relates to signalling and has arisen in  
10 relation to electrical high speed digital communication but is  
not limited to such application.

**BACKGROUND TO THE INVENTION**

Increasingly, very large amounts of data need to be sent  
quickly and reliably, whether between equipments over  
15 interconnection networks or within equipments/installations of a  
basically data processing nature, such as computers internally  
and/or relative to associated units. Massive resources have been  
devoted to speed and reliability of transmission and reception,  
including formats of signals and signalling protocols to  
20 facilitate such communication using electrical and optical  
transmission lines, e.g. coaxial and twisted pair copper-based  
and/or fibre optic cabling. Transmission lines are susceptible  
to signal reflections unless terminations afford a perfect  
impedance match, and impedance is affected by lengths as well as  
25 types of transmission lines involved. Hitherto, signal  
reflections have been seen as a profound problem seriously  
affecting fidelity of signal transmission and reception, and  
justifying great efforts to control them.

**SUMMARY OF THE INVENTION**

30 According to a first aspect of this invention signalling is  
based on deliberate production and use of reflections of  
transmitted signals.

This represents a radical departure from the past. Signal  
reflections are automatic, and deliberate reflections are used  
35 herein for signalling as such, including inherently for two-way

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duplex signalling. There is also highly advantageous further use for control/checking etc purposes with great potential impact on reliability as well as simplification.

Two-way signalling hereof involves first signalling in one-  
5 direction by sending signals with certainty of deliberate reflection thus return signals related to the signals sent according to the nature of the deliberate reflection, and second signalling in the other direction by varying the nature of the deliberate reflection.

10 The source of the first signalling will assess what is received back corresponding to what was sent and determine the nature of the deliberate reflection thus the signalling content. The source of the second signalling needs only to detect what was sent on the first signalling and vary the nature of the  
15 deliberate reflection according to the second signalling.

Basic requirement for binary data communication becomes only for distinguishing between what is reflected for the two binary values ('0' and '1'). For the source of the first signalling, the binary value signals will have different voltage  
20 excursions suited to being assessed as aforesaid. For the source of the second signalling there could be high deliberate reflection for one binary value compared with low for the other binary value, even intendedly near none - but in practice likely some inherent reflection, i.e. effectively accepting reasonable  
25 levels of what much prior effort has gone into trying to eliminate or take to lowest attainable level; indeed, deliberately ensuring much higher levels for signalling purposes. Moreover, actual reflection signals are readily dealt with after it has happened and been received, particularly as part of  
30 control/checking etc use made of it.

This leads to preference for signal formats for the first signalling having successively oppositely-directed voltage  
excursions for each binary value, say with different phase relation to distinguish the two binary values, conveniently anti-  
35 phase relation. If the successively oppositely directed voltage

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excursions for each binary value are of different polarities, and for which the term "bipolar" is used herein, at least reduction of DC signalling component results, down to nominally zero, in practice minimal (subject to transmission path effects) if nominally for the same shape of such excursions.

Specific implementations of signalling hereof involve different signal levels applicable to three phases of bit signals of the first signalling, specifically to extents of excursions and also another level typically between them, preferably to mid-way; conveniently similar opposite polarities and zero for bipolar bit pulses. Advantageously, the bit signal phase with typical mid-way level is a low impedance voltage state rather than the high impedance 'off' state customary for well-known tri-state logic gating.

A second aspect of invention resides in signalling format including prescribed intervals free of actual information signal content, such intervals being sufficient to allow control/checking etc functions to be done, particularly as to signal quality. A nominally substantially constant voltage may apply in such intervals, typically medial of said excursions, conveniently zero and of low impedance nature at least for bipolar bit signals.

At least for bit signals of said first signalling, such intervals can be part of individual signal format for each binary value, say higher excursion of one polarity followed by excursion of opposite polarity and further followed by no excursion; or could be after bursts of bit signals at least where, as is usual, signals in both directions do not interfere, say a number of successive bipolar excursion followed by no excursion.

At least for said second signalling, particular advantage is available for binary value signals if deliberate reflection is by termination means affording extremes of impedance mismatching, namely open-circuit and short-circuit conditions; and automatically applying one as one bit value signal and the other as the other bit value signal. Specific description will follow

of open-circuit termination applied to successively bipolar signals having anti-phase relation to bit values, and voltage value of either bit signal raised up to normally doubled by open-circuit termination and reduced down to normally near cancelled by short-circuit termination. These relationships enable the sources of the first signalling to interpret its received signals as to binary value of the second signal according to which of open-circuit and short-circuit reflections were applied for reflection, say open-circuit for binary value '1' and short-circuit for binary value '0'.

Received signals after reflection actually can indicate correct remote reception of first originally transmitted signals as well as have second signalling binary value readily detected, the correct differences from what was sent being up to voltage doubling and of same shape or down to voltage cancelling.

Moreover, correctness and quality of signalling in both directions are inherently represented by the round-trip nature of the signals after reflection, thus suited to checking only at the source of first signalling. Quality can be investigated to any desired degree or extent albeit only sensibly within the limits of normal transmission characteristics of the connection concerned. This is readily done relative to matching expectations for reflected signals and/or as to shape as such relative to first signalling format, say involving extraction of difference due to reflection as such plus noise. Waveshapes can be thoroughly investigated for total excursion. Checking provisions could, however, be much simpler, including down to reliance on presence detection with any desired thresholding to identify bit values of reflected signals, and checking their sequencing relative to what was transmitted, feasibly without checking of actual timing.

Particularly advantageously, the above successively opposite-going signal formats, permit checking with the availability of double-checking for successively opposite-going nature of signals contents, say as extracted using hybrid means.

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then be variable at will by the transmission equipment, including changing rate within an information bit stream, even from bit to bit; or, and particularly advantageously, for increasing transmission rate to what the preset transmission path will reliably custom, conveniently using an appropriate initial sequence of bits to speed up to failure, then reduce the rate for subsequent information transmission.

These checking and timing features are seen as constituting third and fourth inventive aspects hereof, respectively, whether in generalised or more specific terms.

The above inventive aspects lead to systems with high degrees of virtual internal self-regulation free of at least some of complexities besetting many prior systems in terms of dealing with signal reflections, error detection whether or not extending to correction, distribution of high speed clock timing signals, and making provisions to compensate for attenuation through long runs of transmission line cabling.

In turn, this success by simplification has led to considering another communications system problem, namely addressing provisions so that only target equipment(s) are activated to receive intended transmissions. This is generally achieved by address codes for each equipment concerned and consequent address storing, recognition and transmission provisions being required at each equipment concerned, at least for so-called "ring" or "daisy-chain" systems with each equipment coupled to a side of a common transmission line. Indeed, such ring/daisy-chain systems nowadays attract disapproval in favour of so-called "star" systems that tend to be much less flexible and more expensive, at least for addition of further equipments. The reasons are, of course, closely related to above indicated complexities of very high speed communications systems.

According to a fifth aspect of this invention, routing provisions rely on sending out non-address type signals that nonetheless serve to establish desired connections between transmitting and receiving equipments over communication

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### BRIEF DESCRIPTION OF DRAWINGS

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Figures 1A, B show in-principle transmission line reflection effects for open-circuit and short-circuit terminations;

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SUB BIT

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1. *Chlorophyll a* (Chl *a*)  
 2. *Chlorophyll b* (Chl *b*)  
 3. *Chlorophyll c* (Chl *c*)  
 4. *Chlorophyll d* (Chl *d*)  
 5. *Chlorophyll e* (Chl *e*)  
 6. *Chlorophyll f* (Chl *f*)  
 7. *Chlorophyll g* (Chl *g*)  
 8. *Chlorophyll h* (Chl *h*)  
 9. *Chlorophyll i* (Chl *i*)  
 10. *Chlorophyll j* (Chl *j*)  
 11. *Chlorophyll k* (Chl *k*)  
 12. *Chlorophyll l* (Chl *l*)  
 13. *Chlorophyll m* (Chl *m*)  
 14. *Chlorophyll n* (Chl *n*)  
 15. *Chlorophyll o* (Chl *o*)  
 16. *Chlorophyll p* (Chl *p*)  
 17. *Chlorophyll q* (Chl *q*)  
 18. *Chlorophyll r* (Chl *r*)  
 19. *Chlorophyll s* (Chl *s*)  
 20. *Chlorophyll t* (Chl *t*)  
 21. *Chlorophyll u* (Chl *u*)  
 22. *Chlorophyll v* (Chl *v*)  
 23. *Chlorophyll w* (Chl *w*)  
 24. *Chlorophyll x* (Chl *x*)  
 25. *Chlorophyll y* (Chl *y*)  
 26. *Chlorophyll z* (Chl *z*)  
 27. *Chlorophyll aa* (Chl *aa*)  
 28. *Chlorophyll ab* (Chl *ab*)  
 29. *Chlorophyll ac* (Chl *ac*)  
 30. *Chlorophyll ad* (Chl *ad*)  
 31. *Chlorophyll ae* (Chl *ae*)  
 32. *Chlorophyll af* (Chl *af*)  
 33. *Chlorophyll ag* (Chl *ag*)  
 34. *Chlorophyll ah* (Chl *ah*)  
 35. *Chlorophyll ai* (Chl *ai*)  
 36. *Chlorophyll aj* (Chl *aj*)  
 37. *Chlorophyll ak* (Chl *ak*)  
 38. *Chlorophyll al* (Chl *al*)  
 39. *Chlorophyll am* (Chl *am*)  
 40. *Chlorophyll an* (Chl *an*)  
 41. *Chlorophyll ao* (Chl *ao*)  
 42. *Chlorophyll ap* (Chl *ap*)  
 43. *Chlorophyll aq* (Chl *aq*)  
 44. *Chlorophyll ar* (Chl *ar*)  
 45. *Chlorophyll as* (Chl *as*)  
 46. *Chlorophyll at* (Chl *at*)  
 47. *Chlorophyll au* (Chl *au*)  
 48. *Chlorophyll av* (Chl *av*)  
 49. *Chlorophyll aw* (Chl *aw*)  
 50. *Chlorophyll ax* (Chl *ax*)  
 51. *Chlorophyll ay* (Chl *ay*)  
 52. *Chlorophyll az* (Chl *az*)  
 53. *Chlorophyll aza* (Chl *aza*)  
 54. *Chlorophyll abz* (Chl *abz*)  
 55. *Chlorophyll aca* (Chl *aca*)  
 56. *Chlorophyll acb* (Chl *acb*)  
 57. *Chlorophyll acc* (Chl *acc*)  
 58. *Chlorophyll acd* (Chl *acd*)  
 59. *Chlorophyll ace* (Chl *ace*)  
 60. *Chlorophyll acf* (Chl *acf*)  
 61. *Chlorophyll acg* (Chl *acg*)  
 62. *Chlorophyll ach* (Chl *ach*)  
 63. *Chlorophyll aci* (Chl *aci*)  
 64. *Chlorophyll acj* (Chl *acj*)  
 65. *Chlorophyll ack* (Chl *ack*)  
 66. *Chlorophyll acl* (Chl *acl*)  
 67. *Chlorophyll acm* (Chl *acm*)  
 68. *Chlorophyll acn* (Chl *acn*)  
 69. *Chlorophyll aco* (Chl *aco*)  
 70. *Chlorophyll acp* (Chl *acp*)  
 71. *Chlorophyll acq* (Chl *acq*)  
 72. *Chlorophyll acr* (Chl *acr*)  
 73. *Chlorophyll acs* (Chl *acs*)  
 74. *Chlorophyll act* (Chl *act*)  
 75. *Chlorophyll acu* (Chl *acu*)  
 76. *Chlorophyll acv* (Chl *acv*)  
 77. *Chlorophyll acw* (Chl *acw*)  
 78. *Chlorophyll acx* (Chl *acx*)  
 79. *Chlorophyll acy* (Chl *acy*)  
 80. *Chlorophyll acz* (Chl *acz*)  
 81. *Chlorophyll azaa* (Chl *aza*  
 82. *Chlorophyll abz* (Chl *abz*)  
 83. *Chlorophyll aca* (Chl *aca*)  
 84. *Chlorophyll acb* (Chl *acb*)  
 85. *Chlorophyll acc* (Chl *acc*)  
 86. *Chlorophyll acd* (Chl *acd*)  
 87. *Chlorophyll ace* (Chl *ace*)  
 88. *Chlorophyll acf* (Chl *acf*)  
 89. *Chlorophyll acg* (Chl *acg*)  
 90. *Chlorophyll ach* (Chl *ach*)  
 91. *Chlorophyll aci* (Chl *aci*)  
 92. *Chlorophyll acj* (Chl *acj*)  
 93. *Chlorophyll ack* (Chl *ack*)  
 94. *Chlorophyll acl* (Chl *acl*)  
 95. *Chlorophyll acm* (Chl *acm*)  
 96. *Chlorophyll acn* (Chl *acn*)  
 97. *Chlorophyll aco* (Chl *aco*)  
 98. *Chlorophyll acp* (Chl *acp*)  
 99. *Chlorophyll acq* (Chl *acq*)  
 100. *Chlorophyll acr* (Chl *acr*)  
 101. *Chlorophyll acs* (Chl *acs*)  
 102. *Chlorophyll act* (Chl *act*)  
 103. *Chlorophyll acu* (Chl *acu*)  
 104. *Chlorophyll acv* (Chl *acv*)  
 105. *Chlorophyll acw* (Chl *acw*)  
 106. *Chlorophyll acx* (Chl *acx*)  
 107. *Chlorophyll acy* (Chl *acy*)  
 108. *Chlorophyll acz* (Chl *acz*)  
 109. *Chlorophyll azaa* (Chl *aza*  
 110. *Chlorophyll abz* (Chl *abz*)  
 111. *Chlorophyll aca* (Chl *aca*)  
 112. *Chlorophyll acb* (Chl *acb*)  
 113. *Chlorophyll acc* (Chl *acc*)  
 114. *Chlorophyll acd* (Chl *acd*)  
 115. *Chlorophyll ace* (Chl *ace*)  
 116. *Chlorophyll acf* (Chl *acf*)  
 117. *Chlorophyll acg* (Chl *acg*)  
 118. *Chlorophyll ach* (Chl *ach*)  
 119. *Chlorophyll aci* (Chl *aci*)  
 120. *Chlorophyll acj* (Chl *acj*)  
 121. *Chlorophyll ack* (Chl *ack*)  
 122. *Chlorophyll acl* (Chl *acl*)  
 123. *Chlorophyll acm* (Chl *acm*)  
 124. *Chlorophyll acn* (Chl *acn*)  
 125. *Chlorophyll aco* (Chl *aco*)  
 126. *Chlorophyll acp* (Chl *acp*)  
 127. *Chlorophyll acq* (Chl *acq*)  
 128. *Chlorophyll acr* (Chl *acr*)  
 129. *Chlorophyll acs* (Chl *acs*)  
 130. *Chlorophyll act* (Chl *act*)  
 131. *Chlorophyll acu* (Chl *acu*)  
 132. *Chlorophyll acv* (Chl *acv*)  
 133. *Chlorophyll acw* (Chl *acw*)  
 134. *Chlorophyll*



in-phase (12) and anti-phase (13) reflected signals resulting in transmission line reflection affected signals with voltage respectively doubled (15 in Figure 1A) or cancelled (Figure 1B), specifically shown as 2-volts peak-to-peak as transmitted and 4-  
5 volts peak-to-peak or zero volts as reflection signals.

Figures 2A, B show a preferred signal format for implementing this invention. This signal format involves successive opposite-going excursions at X, Y for each of the binary values for signalling hereof in one direction,  
10 specifically positive first (Figure 2A) and negative first (Figure 2B) for binary '1' and '0', respectively, in respect of bipolar or symmetrical-about-zero sinusoidal waveforms. Figures 2A, B further show at Z a medial level voltage component following each bipolar component X, Y - specifically mid-way  
15 voltage at zero and advantageously of a low impedance nature as produced for use herein.

Signalling in the other direction is according to which of open-circuit and short-circuit terminations are applied, specifically binary '1' and '0' respectively, as described  
20 relative to the drawings.

The inherent purity and smoothness of sinusoidal wave-forms is preferred, but other signal formats could be used with opposite going wave-form shapes, e.g. trapezoidal, triangular, rectangular or variously curved rises and/or peaks and/or  
25 returns. The medial voltage component (Z) could be anything else readily distinguishable from the combined X, Y opposite - excursion components, say if desired to be additionally meaningful; and might be utilised as herein for low impedance zero with any such variation therefrom effectively removed, say  
30 for its desired meaningful purpose.

Application will be considered first in terms daisy-chain interconnection systems of master-and-slave type, see Figure 3 for master equipment 31 and nodes 32 of or associated with slave equipments shown interconnected daisy-chain style between master  
35 31 and passive absorptive termination 35, by transmission line

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parts 33, specifically shown as coaxial cable with signal-carrying central conductors 34 into and out of the master and nodes and outer earth shielding connected together.

Turning to Figure 4, the master equipment 11 comprises a preferably programmable clock source 41 operative at three times intended bit rate, serial data output 42 and input 43 shown afforded by microprocessor 44, output terminating resistor 45 matching characteristic impedance of the transmission line (which need not be coaxial cable), three-level output data pulse generator 46, input receiver 47 with pulse quality checking provision, and virtual hybrid network 48. Electronic circuitry suitable for the illustrated blocks can be implemented with conventional integrated circuit technology.

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The virtual hybrid network serves a similar purpose to transformer hybrid couplers in early telephony, i.e. 4-wire to 2-wire conversion, specifically herein to separate first signalling as transmitted by the master from second signalling by the reflection signals coming back to the master 11 according to deliberate reflection action at the nodes. In addition, associated differential amplifier 481 will have output 482 corresponding to difference in voltage between its inputs 483 and 484. Resistors 485 and 486 have the same value as resistor 44 which matches the transmission line impedance, and will result in the same 2:1 divider action at differential amplifier inputs 483, 484. In absence of any reflection signals, the differential amplifier 481 would have inputs of equal voltage and phase, thus give zero output. However, whatever reflection signal component arrives back at the master from the transmission line will increase or decrease voltage on the line 484 compared with the voltage on the line 483 from between the resistors 485, 486 and output 482 from the differential amplifier 481 will show the difference. In principle, i.e. other than for noise etc, differential amplifier output 482 tracks the reflection components, the transmitted output signal having effectively been removed.

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It does no other processing, but works in a continuous manner, for outgoing and incoming bit signals present on the transmission line at the same time, there being nominally no magnitude and phase difference between outgoing and incoming bit signals and substantially no mutual interference.

This circuit serves for

- termination of incoming waves and preventing reflection from master end - although in principle the energy could be re-used
- launching outgoing master wave sequences towards nodes as the source of all signalling waves
- extracting incoming signal, in this cases, reflected free of any launched signals.

Specifically, Y7 represents 'Phantom signal' source of the reflected bit signal energy from a node as it arrives back at the master; Y9 is signal input (simplex) to launch into the cable from master; Y6 is where returning signal recovered, preferably to be fed to an integrating receiver circuit; Gain seen from Y3 to Y5 is -1 so Y6 kept from moving with outgoing signals. Y5 is input-output port (for voltage such as at centre-conductor of coaxial cable or microstrip etc transmission line;  $Z_0$  represents source impedance of the transmission line (i.e. is not a real resistor); C1 and V4 (inverse of Y9) can be used if

necessary to minimise signal injection into the transmission line; R2, R3 help initial conditions of simulation and are not used in practice; M3 is a reset transistor which is activated whenever the master is outputting a gap period (inter-bit or inter-burst gaps), and helps to restore the self-bias operating point of the circuit while still terminating at characteristic impedance and lets the coupling capacitors adapt to any small DC voltage imposed on the cable by DC supply currents.

Y4 is internal node that slews as C2 gets charged/discharged large C2 means less slewing on Y4; Also, C2 can be small but Y4 should not slew enough to saturate; Y7, R1 represent a 100ohm source; V4/C1 accepts current from V3, C5; C3, C4 and C5, C1 might be lowered proportionally.

And, capacitive divider action (e.g. gate capacitances) acts to reduce feedback around inverter thus lowers transconductance and increases effective resistance, which can be compensated by designing for over-transconductance; changing the attenuation between output port and gate can be used to match to different transmission line impedences under software control; using opposite signal to inject directly at input-output (I/O) node compensates for errors due to capacitive signal currents into I/O node (avoids this path), but at the expense of higher I/O capacitance; opposite signals can be generated from inverters in the ring.

Bit signals used are short symmetrical pulses followed by a zero voltage interval, see X, Y, Z in Figures 2A, B. They have no DC component and allow for entirely AC coupling throughout. The interval Z allows time to interpret the pulse components (X, Y). Figure 2D shows a bit sequence using these bit signals (X, Y, Z), and Figure 2F the same but using a square wave format. Figures 2G, H show application without intervals for groups/bursts of bit signals but with intervals to each side, for sine and square wave forms. The gap signal of Figure 2C is of the same length as a bit signal, but at zero volts throughout; and is used for various control purposes involving strobe and

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reset as below. Figure 2I shows a bit-by-bit interval signal of sinusoidal shape with a large excursion pulse to serve as an end-route indicator, see later regarding routers, and/or for such other purposes as may be desired, including resetting or deliberately breaking neutrality.

5 ~~Sub B~~ Figure 5 shows three-level output data pulse generation for preferred three-level signalling, see fixed clock 51, phase-lock loop 52, selective divider 53, specific divide-by-3 dividers 54A to the phase lock loop 52 and 54B to bit signal format time setting 55, coincidence gate 56 for coordinating bit excursions (X,Y) with input binary data values and controlling production at 10 57 of positive and negative voltages applied to biased base of output transistor 58 through switch 58 controlled by output from time setting 55 to be turned off during the interval (Z) following the bit value representing bipolar excursions (X,Y).

Varying the selective divider 13 enables changing of the bit signalling rate, say to suit practical maximum for the nodes and transmission line(s) of any particular installation, or even specific connection. Such changes can even be on a bit-by-bit basis, see Figure 2E, but are usually on a one-time or periodic system configuration or re-configuration basis. To set such bit rates, the microprocessor 44 is programmed to send at prescribed increasing bit rates until the reflection signals first fail quality testing, then send below that rate as a stored pre-set. 20 In principle, this could be applied to each communication each time it is set up and stored by the microprocessor 44.

Three-level signalling may be inherently less fast than using NRZ (non-return-to-zero) binary code, but has advantages of symmetry and ease of decoding and error checking. Three-level digital systems in use in telephony do not have wave-shape and encoding hereof, such as symmetry with time and amplitude. Also, the third-state hereof is of low-impedance voltage nature mid-way between the '0' and the '1' levels not a high impedance "off" state as Tri-State™ logic gates used for bus isolation. Most of 30

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other digital circuitry hereof operates on conventional two-level binary logic basis.

The third state applies to the interval (Z) and also to the gap of Figure 2C free of data signal as such, which can be used in control of various aspects of operation, including addressing preferably by routing to be described. This interval can be generated by master or slave depending on which is active at a particular time.

Figure 6 shows three-level signal receiving and quality checking provisions for anything from the transmission line. This system can detect errors in each single bit of data transferred with very good dependability, whether for reflections as such or for data signals originating with a slave equipment/node and signalled according to reflection type. It should be appreciated that all signals hereof, including reflections, have at least nominally the same bipolar/plus interval format as true bit signals; and can be investigated as outputs from the differential amplifier 481 associated with the virtual hybrid 48 of Figure 4.

For received bit signals to be accepted as representing binary values '0' or '1', the following checks/tests of its waveform are made.

1. Each received bit signal waveform must be preceded by a gap of at least that between bipolar excursions, see positive and negative threshold detecting differential amplifiers 61A, B (which may conveniently be set at about one-quarter of each nominal peak), inverter 62 and NOR-gate 63 to give positive output whenever both of the outputs of differential amplifiers 61A, B are low corresponding to the received signal being within, i.e. not exceeding, the thresholds concerned as will apply throughout the interval Z and can be counted in data checker 64. This will detect framing errors and general noise on the lines preventing a stable zero reference.

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currents for balance within a fixed percentage, see integrator 66 with log clamp 67 at input and threshold controlled differential amplifiers 68A, B in conjunction with inverter 69 and NOR-gate 70 to data checker 64. The op-amp integrator 66 could be replaced by a transistor with capacitive collector-base feedback.

This check verifies the symmetry of the waveform. Any on-balance unipolar noise pulse occurring during the sample time would leave the integrator with a corresponding non-zero output, whereas any reflection of the symmetrical bipolar component of the bit signal format hereof should closer to zero amount of imbalance even for a wide range of returned signal strengths.

The interval (Z) period should persist for a given time before previous data is accepted, as can be counted in data checker 64. This will detect noise in the interval time.

The above tests give an error if the received signal is too weak and/or for common mode noise voltage.

Instead of fixed threshold levels as shown, it may be advantageous to employ DAC converters to allow adjustment, particularly by software, to facilitate communication for a wide range of round-trip signal attenuation levels. It is also possible to use DAC adjustable response time control of the receive comparators and amplifiers to aid rejecting HF noise if operating at low data rates, say for reliable communication with more distant nodes, as can be achieved by setting of the bias currents in these components (larger currents generally giving faster response with fixed parasitic or added capacitances).

Strobe and reset signals are generated within length of the gap signal of Figure 2C, say strobe in the time Y and reset in the time Z, see delayed pulse generators 71 and 72 in Figure 6, which also shows a fixed delay on output of the NOR gate 63. The comparators 61A,B enable monitoring by the data checker 64 that all interval components (Z) and gap signals (Figure 2C) are within a given range of zero volts, as set by their thresholds.

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Slave nodes 32 reflect signals from the master 31 on a bit by bit basis and on an open-circuit or short-circuit basis depending on bit signal values to be signalled back to the master 31. These reflections are also effective acknowledgements of reception by a node 32 on a bit-by-bit basis.

An alternative receive circuit is shown in Figure 6A, particularly aiding integrated circuit implementation.

This circuit differs from Figure 6, and is based on the integral of the bit signal waveform format is the actual binary value, and that an amplifier that is 'not-fast-enough' produces an integrating response. In Figure 6A:

- Periodic auto-zero-reset of AC amplifiers and integrator overcomes drift, transistor noise, power supply noise expected inside a typical digital CMOS process of small transistor size, as optimised for digital speed. With signalling hereof, inter-bit resets are possible which significantly eases the requirements from drift/noise.
- Each time the reset transistors are activated, amplifiers take up their self-bias voltage and the integrator will be discharged, which has no implications as activated only in gap times and for a short period
- transistor channel lengths can be fairly long to give good gain.
- The same circuit can be used for both node (to get master data directly) and master end (after Figure 4A circuit), bearing in mind that the data this recovers needs interpretation at master.

In operation, M11, M10 acts as a transconductance stage (i.e. Voltage->Current) stage. The input voltage datastream waveform Y6 modulates the gates of M11 and M10. On positive signals above the self-bias point, the Nch transistor conducts more, while the Pch conducts less. - The output point Y3 can then sink current. Conversely, on negative polarity signals relative to the self-bias point, Pch transistor conducts more, and Nch conducts less so can output source current. At the self-bias point, M11 and M10 currents are the same, so no net current

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available at Y3. Y3 feeds a low impedance point as input to integrator, and the voltage at Y3 changes very little ( $\pm 90\text{mV}$ ), so there is highly integrating effect and the parasitic feedback capacitances do not come into play. M7 and M8 act as Integrator. In contrast to M11, M10 the output voltage here at Y7 is allowed to slew. No feedback capacitor is shown, nor is needed to implement the integration function because the parasitic Drain->Gate capacitance provides this at low signal swings. The signal at Y7 is approximately the integral of the input. For example for the first '1' bit signal wave coming in, Y7 integrates positively while the input wave is positive. At zero-crossing of the input wave, Y7 is at its peak. During the second (negative) half of the bit signal wave, Y7 integrates downwards. The total area under the positive half of the wave will equal that of the negative half of the wave for end of the bit signal time to be return to the self-bias point. At higher Y7 signal swings, as for slow rate input data, the output at Y7 can swing towards either one of the supply rails. When this happens, the mosfet connected to that supply rail goes from saturation with drain end pinched off to ohmic with drain end connected ohmically to source. When this occurs the Drain->Gate capacitive feedback increases to be the full Gate oxide capacitance. This effect is very useful because it makes for an integrator with high swing, good sensitivity but a very large charge ultimate charge capacity, making the circuit useful to integrate over a 10:1 time range. Due to charge conservation, all charge stored on the mosfet must be removed. Only when all charge stored during one polarity of the input waveform is removed does can Y7 go back to mid-point - just what is required with balanced input signals. Digital extraction of the waveform at Y7 is done with M2/M3 to detect '0's and with M4/M6 to detect '1's (output pulse sense being inverted). Thresholds are set by the relative channel widths of transistors M2 and M4 relative to those of M7, M11. M2 is narrow to give the inverter a lower-than-normal threshold, M4 is wide to give that inverter a higher-than-normal threshold.

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Use of transmission line transformer allows good DC path with low parasitic elements as transmission line construction effectively makes stray capacitance and leakage inductance become the transmission line. The transformer can also with advantage be arranged to perform impedance conversion and single/double ended conversion (balun function). This would be useful for converting the signalling medium between coaxial (unbalanced) and twisted pair (balanced) cabling systems.

Inherent inversion of the through data (both ways) need not cause problems as the master 31 can easily, by software control, invert all it's output data according to the node connected, actually alternately so for ring or daisy-chain configurations. Similarly, reflective signals will alternate in sense for odd and even numbered nodes and this too can be inverted by software control - though not necessarily required when compared to sense of transmitted wave forms.

The described system may be summarised by:

- '1' waves and '0' waves only interpretable directly by the node from the arriving master data.
- Node reflector termination is controlled by second signalling data the node wants to send, i.e. with no reference to prior or currently-arriving data from master.
- Master can sort out what it means with reference to what it sent
- Node reflects complete waves, both the high and the low phases in an order depending on first signalling bit value
- Node reflector termination changes state before each new master bit signal arrives
- Node receives one bit signal first from the master data at the same time as reflecting a second signalling bit (independent) back
- The 'short circuit' termination condition cannot really be zero Ohms or else the node cannot detect what master is sending in this condition, so in practice maybe 5x less

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than characteristic gives good reflection and allows a small master signal to be detected and resolved.

- The '1' and '0' as detected back at the Master end receiver are not useable without reference to what the master sent but are readily sorted out from conventionally stored bit values taken in order.

From one somewhat mathematical viewpoint relative to mosfets: if a node has a '1' to send to master, it signals this by multiplying the incoming master bit signal wave by +1 when making the return reflection (open circuit reflection does this, e.g. as Nmos=off). If it has a '0' bit to send to master it multiplies the master wave by -1 (short circuit reflection does this i.e. Reflector Nmos=on). Master sorts this out - to get the binary value the node was sending - by figuring out what the multiplicand was, i.e. +1 or -1. This can be done by multiplying the original binary value sent by master sent by the apparent binary values that came back, on a bit-by-bit basis. Effectively, master solves - [Master Bit sent] X [Unknown] = [Raw bit Received] - which can be simply resolved using an Exclusive -OR gate, or software instructions acting on memorised value of what master sent.

A transformer is not the only feasible way of linking two RF ports with either High or low impedance RF path. A power mosfet or npn-bipolar transistor switch (or other type of semiconductor or electromagnetic switch, e.g. relay) could be used to achieve this purpose.

For systems not needing DC or lfAC electrical supply (e.g. where supply is already available) an entirely monolithic integrated system can be provided using P-channel or N-channel mosfets as switches to connect or isolate one RF port from the other, and to induce "open circuit" reflections or "through" connection as required, see P-channel mosfets 101, 102 in Figure 10. Standard means of charge injection cancellation would limit spurious signals created during switching.

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Figure 11 shows use of bipolar transistors 111, 112 and 113 together with alternative to analogue switch element with a series resistor for the short-circuit reflections allowing detection of the incoming waveform signal with simultaneous short circuit reflection of incident waveforms. When RF switch 114 is Off, the emitter follower transistor 111 is turned Off, the base is reverse biased and the emitter current sink transistor 112 is also turned Off by 0v on its base. The emitter circuit plus collector for transistor 112 represents a very high resistance in parallel with some small stray capacitance to ground. Resistor 115 provides reverse base bias being typically at least 10Kohms for specific example involving bias level of +2v and related through monolithic devices to +2.6v as follows. When the RF switch is Off, AC signals coupling via capacitor 116 experience very little attenuation or reflection since resistor 115 is high and emitter of transistor 111 is reversed biased. In the Off condition, the switch can handle signals of 5 volt peak-peak before TR1 emitter becomes forward biased.

To turn the RF switch On, the switch control line goes to +2.6v, which very quickly turns On transistor 111 and slightly later, the current sink pair 112, 113. With correct timing it is possible to ensure that there is very little change in voltage at emitter of transistor 111 nor spurious output into source impedance, as the ultimate emitter voltage is also 2volt (2.6v -  $V_{be} @ 0.6v = 2v$ ). In the On state, the emitter current of a bipolar transistor gives an effective output resistance of  $25/I_c$  (in mA) or 5 ohms at 5mA  $I_c$ . This is adequately low relative to source impedance to produce strong short-circuit reflections of waves on the transmission line as source impedance. The switch is turned on or off only outside bipolar bit value signal components, so as to limit spurious signal injection. Resistor 117 is added for collector of transistor 112 so that analogue of the master signal appearing as a modulation of emitter current is available for the node to be able to receive the master data even

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when the wave is to be short-circuit reflected, the RF voltage and emitter being at zero.

Present silicon technology effectively limits npn-bipolar transistor provision of Figure 11 to operation up to about 500 MHz. Higher frequencies of operation up to 1GHz are feasible using gallium arsenide monolithic microwave integrated circuit technology to fabricate switches, see 121 and 122 in Figure 12, as optionally driven PIN diodes, say with integrated gallium arsenide laser provision 113 on the same substrate as a single monolithic device. Typical on/off switching times can be as low as 0.1 ns.

At very high data rates (e.g. microwave) use could be made of PIN diodes incorporated into hollow metal waveguides of an microwave circulator arrangement to facilitate routing.

Further regarding node provisions and circuitry, short-circuit reflection at transformer mid-point is feasible using previously indicated circuitry design. However, as the on/off times are not critical for such switch, a simple saturated NPN transistor switch could be employed and would conveniently pass DC current as may be desired for power.

Three-level detection for the node may be simplified, as all data pulses sent to the node during communication are reflected (in one way or another) back to the master where they are tested for noise pickup. If "round-trip" pulse quality is satisfactory it seems reasonable to assume that included one-way pulse quality must be acceptable. On this basis, the simplest node needs no additional error detection and correction logic.

A saturated JFET or mosfet or bipolar transistor can be used to extract some operating current from the transmission line and still present a high AC impedance transmission line - and signals might also be incorporated into above centre-tap transformer RF reflection switching. Alternatively, for high power levels an RF inductor could be used to extract significant DC current for powering local electronics or actuators and still present a high AC impedance. Low frequency AC power is also

possible (50Hz, 60Hz) as this is well below the normal signalling frequencies thus isolated by the small coupling capacitors of the signalling circuits.

Node operation involves initial master output quiescent (interval/gap state Z) and it is assumed that this has persisted for longer than a reset time period, so all nodes have been reset. Then, as for Figure 7, all nodes will be set (switch 72 On) to reflect the first incoming wave with short circuit termination to produce anti-phase reflection of the first bit signal from the master which will assess the anti-phase reflection signal as above effectively separated out by the virtual hybrid 48. If satisfactory, the master can continue to send and receive data with the node at full duplex capability.

In Figure 7, node sampling at points numbered '1' and '2' corresponds to short-circuit and open-circuit termination, thus anti-phase and in-phase reflection, thus small and large reflection signals, all respectively signalling from a node to the master involves anti-phase short-circuit reflection switch 72 being on when sending binary value '0' as in Figure 2B. Sending binary value '1' involves setting as for in-phase open-circuit reflection, specifically have both of switches 72, 73 off. If an incident wave pulse from the master appears at the node, the series inductance of the wide-band transformer, now acting as an inductor (see winding polarity dots), presents a high impedance and so little if any energy is coupled through and on to other nodes - as inductor current cannot instantaneously change and wave-shapes from the master have very high frequency components only.

For every bit of data received by the node via the three-level detector to extract the bit (and set a clock), one bit of node data is returned to the master and the system can operate in a full-duplex mode. Reflection control switches 72, 73 can be changed over only during the quiescent interval/gap times of master pulses, so switch at zero voltage and minimise spurious signal injection. At no time can any meaningful signal pass the

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node that is active, so nodes further down the transmission line from the master get very little if any signals - effectively being reflectively isolated.

As each master transmitted bit signal is received, say shifted  
5 into receiving register of the node, the next bit of node data can be sent back, typically clocked out of the sending shift register of the node.

In principle, the master always receives back exactly the same bit signals as it sends - automatically, by reflection and as  
10 retrieved at the master for quality checking as above, the reflection signals further representing node data by nature of termination and reflection caused. Checking interpreted binary value of each received bit signal as compared with binary value of what was transmitted enables the master to determine the  
15 binary value of the bit signal from the node - same bipolarity means the node did in-phase open circuit reflection so was sending a logic 1, and reversed bipolarity means short circuit anti-phase reflection so the node sent a logic 0.

Because it is fundamentally the same bit signal format used to  
20 transmit and receive data, quality checking at the master on received signals will confirm absence of noise, including on round-trip signals, thus give good indication of data integrity both ways.

A useful selection mechanism arises in relation to use of  
25 reflections by a node to send all data bit signals to the Master without nodes further down the transmission line getting any signals. After arbitrarily long two-way data transfer is complete with any node, special gap intervals can be inserted in the output of the master. A short gap, typically 500 ns, can serve  
30 as a strobe to end communication with the currently addressed node. On detecting this strobe condition, the node ceases to reflect any more signals simply by turning switch 73 off and RF 72 on, which makes the wide-band transformer act as true 1:1 inverting transformer and solidly couple the input and output RF  
35 ports in a bi-directional manner - due to common point of the

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node is to be reset, thus re-activating the node for selection by the master, i.e. for anti-phase reflection of next incoming master bit signal. If the master keeps the selected data route busy with data signals and short strobe gaps de-activation nodes cannot even be selected, i.e. stay de-selected until there is a preset gap.

A node might also generate a signal like this during normal duplex data transfer after being properly addressed, say to indicate to the master a critical condition mid-way through a long data transfer, e.g. buffer full, data error etc.

In customary two-way data transfers with the nodes on a sequential polling basis, through to the last node concerned, master uses a reset gap to reactivate all the nodes, typically for a new selection sequence.

No additional selecting/address mechanisms, e.g. identifier codes, such as serial numbers or addresses, or software protocols are required for unique selection and communication with any node anywhere in the system.

Such sequential selection scheme can be extended to provide a useful network feature, say for digital TV distribution and/or videoconferencing, where it is desirable to send the same data to multiple nodes simultaneously. If the state of the bit signal first sent to a node was latched as well as anti-phase reflected, and if this state corresponded to binary value '1', then after the strobe period, all nodes addressed with the same binary '1' signal could still be enabled to receive the data. Nodes not intended to receive the broadcast data would be addressed with a binary '0' bit signal.

The master could so select nodes right through to the customary final passive terminator, then begin to send data on a broadcast basis to all the selected nodes. Operation would be in half-duplex mode as none of the nodes addressed for broadcast should try to transmit own data back to the master, so can present one termination continuously. Each node needs only an

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indicator that it is odd or even and to make a one-bit comparison.

Interestingly, multi-speed operation capability of three-level systems hereof itself allows a form of selection, as nodes with slow AC response will automatically significantly attenuate transmitted data below the receive threshold. Indeed, attenuation by cabling can also prevents low speed nodes from ever seeing high speed data at the end of the transmission line.

Examination of the circuit diagrams of the drawings reveals a good DC current path right throughout the network. This path begins at the master end and passes through the transformer windings and returns through braid of coaxial cable or other conductor for twisted pair or microstrip. This enables supply of DC or low frequency AC power by way of the transmission line itself.

Implementation of systems of this invention is also viable for interconnections more complex than daisy-chains or rings, see for example a so-called internet of which Figure 13 shows a part involving more than one master (M), many nodes (X) in several branches, and router provisions at junctions between branches.

Figure 14 shows a node modified for accessing and communication from either side of its transmission line connections, as would, of course, be desirable even for true ring networks. Figure 14 shows three RF reflector switches 141, 142, 143 and four coupling points (A-D), along with consequential two-wave data in and three-way out switching provision 145 according to signal source and additional logic 146. When in communication with a master unit from one side, the other side is effectively 'locked out' as the node is configured for constant reflection (either open or short circuit) to the master concerned. In both these cases, series inductance of the broadband transformer 147 presents an AC "open circuit" condition to a master trying to access an 'engaged' node from the other port no matter if the node is reflecting open-circuit or short-circuit to the master in control.

5                   Simultaneity of attempted access to a node is unlikely as  
there is only a very short time period for node switching. If it  
happens, received quality errors by the master that loses out  
will soon disclose that a line of nodes is engaged beyond the one  
last active or addressed. A master could retry a node until it  
10 becomes available by repeatedly sending bit signals to it until  
the reflection signal changes from that for "engaged", as would  
happen after the other master had sent a node reset by going  
quiescent for the reset period and re-activating the node for  
selection.

Routers have been developed with valuable features for a combination "ring" and "star" topologies as well as Internet topologies, particularly as to allowing expansion in the number of nodes connected without exposing the data pulses to many spuriously reflective interconnections (as for all the nodes in a long line or loop), and as to providing 'bypass' relative to strings of nodes for any reason, say if using or benefiting from dedicated cables.

The router of Figure 15 is made up mainly of components and  
35 blocks already described so description is concentrated on

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path of the router, all the inputs are returned to characteristic (absorb, i.e. non reflect) termination resistance and the router is available for control by the first master signal to arrive on one of the three ports.

5 Other hardware or software logic features including allowing the router to make its characteristic impedance termination persist for a particular port to furnish a convenient termination when using above broadcast feature, and/or to detect when a master sends a routing direction signal is followed by a  
10 strobe (which it would not normally do).. A unique bit signal can cause the router to hold or restore the characteristic termination impedance for the input port, say ignore the route selection just specified. The other two ports could still be switched together by master signals on either one of those ports,  
15 the 'engaged' signal being returned only should an attempt be made to route onto the port with the persistent characteristic termination. Reset condition detected has the characteristically terminated port can clear all the engaged logic and return the port to normal operation.

20 DC or low frequency AC power can be applied to the network at routers to maintain a good low resistance supply of power to the nodes and other equipment attached.

Such routers can facilitate large interconnected arrays of nodes and facilitate redundancy in possible paths between nodes,  
25 for which selection paths can 'snake' around the network. If one path is found to be inoperable or engaged, an alternative selection path could be tried without needing any complex or expensive electronics or software.

Figures 15A,B show advantageous router  
30 reflection/switching. In Figure 15A, voltage levels are centered around ground and low excursion to be compatible with Nch mos switches and routable through modern CMOS Ics without causing latch-up as bulk CMOS cannot accept large negative inputs. Actual ground, not AC ground, can now be used to terminate  
35 reflection transistors thus avoiding large capacitors and

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Ultimately the master reaches the end of the "All '1's" path through the network to a passive termination of characteristic impedance recognisable by signal absorbing without the no-reflect gap condition. The master now knows many nodes  
 5 are on each part of this particular 'All 1's' route through the network plus the locations of routers up to the end of the path. Network investigation continues iteratively by the master first re-running the same sequence up to the last router then sending a  
 10 '0' bit signal to investigate the branches off the last leg of the previous route. The master iterates until it has fully explored every branch and chain of the network to build up an internal network map of nodes, routers and terminations.

For complex internet arrangements with multiple masters, network investigation may lead one master to find another, at  
 15 least assuming the other master is quiescent. Masters can have software protocol so that they recognise each other, preferably also share information. This could be a basis for a parallel processing system.

Application is envisaged to parallel processing up to  
 20 supercomputer architectures using large multi-bit bus systems where say 32 or more parallel channels of this system can be used (e.g. on microstrip media), and the nodes could actually be of so-called "wide" parallel input nature for peripherals or memory. Signal routers can be also extended to 'n' bits.

25 Conventional data bus topologies (e.g. PCI bus, VME bus, NuBus) only allow one bus "owner" to control the bus at any one time. Total bus bandwidth is fixed and does not grow as more peripherals wide nodes are added. Systems of reflective isolation proposed herein are applicable between adjacent sections of bus  
 30 and 'engaged' signalling lets every section of a bus be split and operated point to point at the full data rate. Cards which interchange large amounts of data with each other can be located adjacent in the bus. A single 'master' program is still able to communicate with the cards individually if periodic 'idle' slots  
 35 are inserted.

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in a line since any deviation from nominal impedance (higher or lower impedance) caused by a short circuit or an open circuit results in a reflection. Also, when a coaxial cable is crushed or stretched badly it experiences a measurable change of characteristic impedance and therefore gives reflections.

A master hereof typically includes a programmed computer which can easily detect and store the presence of a new node the next time a full network explore is performed. With time domain reflectometry included, a new detected node can have its position (in electrical length units) determined by the time of flight of a bit signal. A router can be added at any point to expand the system. Multi-way routers with internal terminations can be used to allow for such as a 8 port "extension socket" type cable into which equipments can be plugged.

When getting data from far distant nodes at high speeds, a full duplex operation may not be practical. The problem arises from the fact that spurious reflections from master output signals by in-between nodes and cable and/or connector mismatches can give a return signal in which the reflected signalling energy from the node can be swamped by the spurious reflections. One remedy would be to reduce the data rate as reflections reduce with operating frequency esp. stray capacitance reflections. Another would be to have the nodes able to generate their own wave-shaped three level outputs and include a local clock generator of variable frequency to suit cabling, on every node so clock pulses by the master were not present during reading of data from the node - though this is seen as undesirable from the aspect of cost, complexity, power consumption and the inevitable protocol overhead probably requiring local software.

Help is now proposed for this problem, keeping the nodes as simple as possible. The basis is that whatever actual transmission line connection is concerned its spurious signalling effects are inherently of a substantially constantly repeating nature for each bit signal hereof including its reflection. This spurious content is actually the extent to which there is

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difference from exact matching in the identifying comparison hereof. Perhaps ideally, that would be stored as output from the relevant differential amplifier for prescribed known test bit signal transmissions and reflecting and read back synchronously as a correction for each received signal. However, that is too complex to consider trying to do when the whole rationale of this invention is reducing complexity in favour of simplicity, though a charge-coupled-diode analogue memory could well be practical. Instead, advantage is sought from the fact that it would be equally effective to hold bit signal versions complete with spurious effects, and compare them with the incoming reflected signals. A successful practical approximation of this has been achieved using a length of coaxial cable as a kind of memory device for actual reflected signals, see Figure 17.

The coaxial cable length is such that an exact multiple of the bit signals will traverse it twice - from input to a fully reflective termination and back - at the transmission bit rate of the system. For a nominal 200 Mbps transmission rate using  $3 \times 1.66 \text{ ns}$  per bit signal a coaxial cable length related to 12.5 Mbps would hold sixteen bit signal wave-lengths. For good coaxial cable rated at 0.8 of speed of light, required coaxial cable length 10 metres.

The input node is zero volts for any arbitrary regular waveform at 12.5Mhz and multiples thereof. For example, considering the leading positive edge of a regular square waveform that will travel down and return as leading negative edge of a pulse of opposite polarity in transit time 80ns, so a repetitive wave-form of period 80ns will have a rising edge at the coaxial input/output node at exactly the same time - so will input and reflected voltages will cancel as the series drive resistance into the coax matches the wave impedance of the reflected wave (assume output impedance of transistor concerned is zero). This cancellation will persist for the entire positive excursion of the square wave, and further through the negative excursion, and so on - and applies to any waveform repetitive

within a time period integer divisible with no remainder into the round-trip time in the coaxial cable memory hereof, see 161 in Figure 17 for which there will be inversion of reflected voltage but same magnitude going back towards the input/output node.

5 There will also be rejection of non-perfect CMRR of the receive amplifier.

The operating frequency can be of a voltage controlled nature and set by actual response of the coaxial cable. The RMS voltage (rectified power monitor) of the receive signal can be a digitised variable known to the master controller.

When fetching data from a node as required, the master will work in half duplex mode, and send pulses to clock the remote node that are of constant binary wave values - either a constant stream of '1' or of '0' wave-forms. These pulses are repetitive within the round trip time of the coaxial cable memory 161 and reflections from these output pulses can be used to prime the memory 161, resulting after sixteen pulses and full traversal of the network path concerned in cancellation no matter what the phase relationships of the individual sources of spurious reflection and how they combine.

The master can periodically route regular waveform directly into the coax memory for a tune-in period and frequency can be adjusted using a DAC driving a varicap oscillator until reflected power measured at the coaxial memory entry is minimum, i.e. the system self tunes to suit the coaxial memory.

When the coaxial memory is primed and the node begins to output data with short-circuit or open-circuit reflections same at the master receiver will also go to the coaxial memory drive amplifier. The coaxial memory may produce cancelling or additive effects as what is streaming back out of the coaxial memory entry point is cancelling only the repetitive unwanted signal. A very clean reproduction of the desired signal can result with the repetitive noise.

The first pulses will be checked by the three-level detection circuit and pulse quality logic as per normal. For

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from the communicating node. An alternative would be to use a high speed DAC output to subtract using analogue summing amplifier from the received signal to leave the desired signal.

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